An Auto-input-offset Removing Floating Gate Pseudo-differential Transconductor

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ABSTRACT

A floating-gate pseudo-differential transconductor is presented, in which the differential input signal is allowed to have a dc offset. Normally such an offset would render a normal CMOS differential pair useless. The circuit inherently removes any dc offset from the floating gates by feedback mechanisms involving Fowler-Nordheim electron tunneling and hot-electron injection. This technique can enable direct cascading of several cells without amplifying and accumulating offsets, or can be used to generate differential current mode signals from a single voltage source that has a dc offset, as with an electret microphone.

1. INTRODUCTION

Designers of analog integrated circuits often find dealing with offsets challenging. The conventional approach of using large blocking capacitors in conjunction with resistive elements is unfeasible for single-chip designs, as these require unrealistically large areas for large time constants. Other schemes include intricate feedback loops for compensating of the offsets or complex clocking schemes [1], periodically calculating and subtracting the offset.

Floating gate transistors have a conducting gate encapsulated in a high quality insulator such as SiO₂. Charge can be removed or added to the floating gate by three mechanisms – 1) Increasing electron energy by UV light, 2) Using Fowler-Nordheim tunnelling [5] and 3) Hot electron injection. The last two mechanisms can be used to adjust the charge on the gate dynamically [2] [3] [4].

NMOS device hot-electron injection [2] [3] [4] [7]:

In this process electrons near the surface of a semiconductor acquire more than about 3.2 eV of energy, typically by being accelerated in an intense electric field, such as that produced in devices operated in the weak inversion region. 3.2eV are enough to surmount the silicon/silicon-dioxide barrier and so once in the silicon dioxide conduction band, an electric field applied across the oxide can carry these electrons to the floating gate. In order to make the drain-gate electric field favour hot

Figure 1: The auto-input-offset removing floating gate pseudo-differential transconductor. The negative feedback is provided by the physical mechanisms of electron tunnelling and nFET hot-electron injection.

electron injection, the threshold voltage of an NMOS transistor is raised, by increasing the doping of the substrate. This is achieved by violating design rules in a true twin-well process by placing a PTUB directly on a p-substrate and placing a normal NMOS device on this highly doped substrate. Alternatively in a BiCMOS process the bipolar base dopant can be used to increase the substrate doping [4]. The hot electron injection gate current increases linearly with the source current, over the whole of the sub-threshold range, when V_{db} and V_{gb} are held constant [6] and is exponentially dependent on the drain-source voltage. The current due to this mechanism can be modelled using the following form:

$$I_{inj} = \beta I_s e^{\left(\frac{V_{dc}}{V_{inj}} \right)} \quad (1)$$

Where I_{inj} is the hot-electron injection current, I_s is the device source current, V_{dc} is the drain-channel voltage and β , V_{inj} are fit constants.

Fowler Nordheim Tunnelling [5] [7]:

The quantum mechanical nature of electrons i.e. the wave nature, allow an electron to have a finite probability of crossing what was once thought of as an impenetrable oxide barrier. The probability of crossing the oxide, and hence the effective current can be increased by increasing the electric field strength across the barrier. Hence, using a Fowler – Nordheim form the tunnelling current can be modelled using the following form:

$$I_{tun} = I_0 e^{-\frac{t_{ox} \epsilon_0}{V_{tun} - V_{fg}}} \quad (2)$$

Where I_{tun} is the tunnelling current, I_0 is the pre-exponential current, t_{ox} is the oxide thickness, ϵ_0 is the electric field strength, V_{tun} is the tunnelling voltage and V_{fg} is the floating-gate voltage.

By taking advantage of these mechanisms the pseudo-differential floating-gate transistor presented can be driven with differential signals with considerably large, slowly drifting, dc offsets.

Figure 1 shows the auto-input-offset removing floating-gate pseudo-differential transistor.

2. QUALITATIVE OPERATION

The circuit consists of a pair of source connected floating-gate NMOS devices with a diode-connected FET (Q7) to provide the sinking current. The floating-gate devices have increased substrate doping to improve the hot electron injection efficiency. Each branches output currents are mirrored by the top-end current mirrors (Q3 - Q6). This basic cell may be used to make a number of different circuit elements i.e. an op-amp, a driver for current mode differential circuits, etc.

The diode-connected FET serves two purposes. Firstly it provides the necessary feedback to realize a pseudo-differential behaviour between the two floating-gate devices. Secondly, it provides adequate compression at the common-source node to delay the hot-electron injection mechanism, hence increasing the settling time-constant.

The drain currents and tunnelling voltages are set such that, at the circuit's steady state operating point, i.e. $I_1 = I_2$, the electron tunnelling and hot-electron injection currents balance one another. The complimentary nature of these mechanisms provides the necessary negative feedback to restore the steady-state dc operating point if a disturbance occurs. In other words, if the floating gate voltage decreases, the electron tunnelling mechanism becomes more dominant, causing the voltage

to increase. Likewise, if the floating gate voltage increases, the hot-electron injection current would be the dominant, causing the voltage to decrease.

The auto-offset removal action occurs as follows:

1. A slowly changing differential signal will have the effect of changing one (or both) of the floating gate voltages.
2. The two drain currents will change in opposite directions, i.e. if I_1 increases then I_2 will decrease. This is due to the action of the shift in the common source voltage of the floating-gate pair.
3. The devices source voltage will be changed; hence the gate-source and drain-source voltages will also change. This will cause an imbalance between the electron tunnelling and hot-electron injection mechanisms.
4. This imbalance will result in charge transfer; either to or from the floating gates, thus adjusting their voltages back to their quiescent steady-state values.
5. Therefore, the two drain currents will also return to their quiescent operating points, despite the inputs having a dc offset or low frequency drift.

3. QUANTITATIVE OPERATION

DC Analysis:

Under steady-state conditions, i.e. $V_{in(+)} = V_{in(-)}$, the output currents are equal and therefore the floating-gate voltages must also be equal and constant. For this to occur the net charge on the floating-gates must remain unchanged, which implies the mechanisms of electron tunnelling and hot-electron injection balance one another.

$$I_{tun} - I_{inj} = 0$$

$$I_0 e^{-\frac{t_{ox} \epsilon_0}{V_{tun} - V_{fg0}}} - \beta I_{S0} e^{\left(\frac{V_{dc0}}{V_{inj}}\right)} = 0 \quad (3)$$

Applying Kirchoff's Current Law (KCL) at the floating-gate node forms the following relationship.

$$C_{fg} \frac{dV_{fg}}{dt} = C_{in} \frac{d(V_{in} - V_{fg})}{dt} + I_{tun} - I_{inj} \quad (4)$$

Where C_{in} is the input capacitance, C_{fg} is the total floating-gate capacitance, V_{fg} is the floating-gate voltage, V_{in} is the input voltage, I_{tun} is the tunnelling current and I_{inj} is the hot-electron injection current.

On applying an input signal, the contribution of the electron tunnelling and hot-electron injection currents can be considered as negligible, yielding:

$$C_{fg} \frac{dV_{fg}}{dt} = C_{in} \frac{d(V_{in} - V_{fg})}{dt} \quad (5)$$

This indicates that applying a relatively positive input voltage will cause an increase in the floating-gate voltage. Consequently the source voltage will also rise due to an increase in current in the diode connected FET. This will result in the following conditions:

$$V_{fgs0} < V_{fgs1} < V_{fgs0} + \Delta V_{fg} \quad (6a)$$

$$V_{fgs2} < V_{fgs0} \quad (6b)$$

Reviewing the net gate current (current into the floating gate) gives the expression:

$$I_g = I_{tun0} e^{\frac{V_{fg} - V_s}{V_{th} - V_{fg}}} - I_{inj0} e^{\frac{V_{fg} - V_s}{nU_T}} e^{\frac{V_d - V_s}{V_{inj}}} \quad (7)$$

Evaluating the above conditions (7) into this expression (8) yields:

$$I_{g1} < 0 \therefore \frac{dV_{fg1}}{dt} < 0, \quad (8a)$$

$$I_{g2} > 0 \therefore \frac{dV_{fg2}}{dt} > 0 \quad (8b)$$

The imbalance due to these mechanisms will bring the floating-gate and source voltages back to their quiescent steady-state values at which the equilibrium will be restored.

AC Analysis:

For small signals the model shown in figure 2 can be used as an approximation to the floating-gate input devices. [4]

Figure 2: The small signal model for an NMOS floating gate device.

Analysis of this model yields the following small-signal voltage transfer function between the external input and the floating gate node:

$$A_v = \frac{V_{fg}}{V_{in}} = r_{fg} \left[\left(1 - r_{fg} r_0 g_{fg} g_m \right) \left(r_{fg} + \frac{1}{2\pi f C_{in}} \right) \right]^{-1} \quad (9)$$

To solve (9), the following substitutions are made: $k = (1 - r_{fg} r_0 g_{fg} g_m)^{-1}$ and $X = 2\pi f C_{in}$ which reduce it to:

$$A_v = \frac{V_{fg}}{V_{in}} = \frac{k X r_{fg}}{1 + X r_{fg}} \quad (10)$$

Evaluating this expression gives the high-pass 3dB roll-off at: $f = 21mHz$. This value is consistent with the simulation results shown in figure 5.

4. SIMULATION RESULTS

The following simulation results have been obtained by creating AHDL tunneling and hot-electron injection models adapted for this particular 0.8 μm process from those extracted by Diorio et al. [2] [3] [4].

This auto-input offset removal mechanism is illustrated in figures 3 and 4.

Figure 3: Simulation results for a dc step on the Vin(-) input. This illustrates the feedback mechanism by which the steady-state quiescent operating point is restored. The operation of devices Q1 and Q2 are shown in the left and right plots respectively.

In figure 3, a DC step is input to Vin(-) whilst Vin(+) is kept at a particular voltage. Consequently, an imbalance in the tunneling and hot-electron injection currents is shown

in the second row. This causes the disturbed floating-gate voltage to drift towards its original value, shown in the third row. Finally, the output currents follow the trend, shown in the bottom row.

Figure 4: Simulation results for the auto-input-offset removing floating gate pseudo-differential transconductor to a voltage pulse superimposed onto a 3Hz sinewave. The results (from top to bottom) show: (i) input voltages, (ii) tunnelling and hot-electron injection currents, (iii) source and floating-gate voltage for device Q1 and (iv) output currents.

5. DISCUSSION

This paper introduces the concept of the auto-input-offset removing floating gate pseudo-differential transconductor based on the mathematical equations that model its components. Its ability to remove any dc offset has been successfully demonstrated, through simulation. The system assumes matching of tunnelling and injection devices. As indicated by the work of Millard et al. [8], the use of tunneling and hot-electron injection will deteriorate the matching. For demanding applications, some form of feedback to the individual tunneling voltages may be required. However as technologies scale, the required tunnelling voltages are reduced and the quality of the oxides become better allowing for greater matching.

Also, as DiMaria et al. [9] have indicated, continual hot carrier injection and tunnelling will result in degradation of the oxide quality. Therefore when setting the tunnelling voltage (electric field strength) and floating-gate drain current (hot-electron energy,) they should be kept to a minimum in order to minimize oxide degradation effects.

The use of a diode-connected device attached to the common-source node means that common-mode small signals are not rejected; however these may be removed by using a classical differential pair as the next stage.

Assuming a cascaded structure of independent amplifiers the offsets should have a zero mean and these are removed at every stage the resulting offset should be similar in magnitude to the individual devices.

Future work can concentrate on using more advanced models in addition to dealing with practical issues such as layout and device matching.

The circuits' sensitivity to process variation can be determined, which could result in models suitable for fabrication.

Figure 5: Simulation results of ac analysis showing the high pass characteristic. The 3dB roll-off is at 24.7 mHz.

6. REFERENCES

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